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Fabrication of 3D Silicon-based Photonic Crystal Structure with "Single" Self Aligned Etching Process

by Gerard Dang, Monica Taysing-Lara, and Weimin Zhou

ARL-TN-0407 **September 2010**

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14. ABSTRACT
We have designed and developed a simplified three-dimensional (3D) photonic crystal (PhC) fabrication technique that can be used to fabricate a nanoscale 3D structure from the two-dimensional (2D) surface of a silicon (Si), or silicon on insulator (SOI) wafer with a "single" modified Bosch plasma etching process. Using this technique, we demonstrated such a PhC structure that includes hollow-core waveguides with high-contrast gratings as cladding. The etching process produces deep trenches with controlled width variation along the vertical direction. This method uses only a single mask (such as e-beam lithography mask) without alignment, and there is no need for deposition, regrowth, etc. This technique may greatly reduce the fabrication cost and increase the yield of 3D PhC devices.

15. SUBJECT TERMS
Photonic crystal, Silicon, waveguide, nanotechnology

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1. Introduction

High contrast gratings have been explored by C. Hasnain as a replacement for the distributed Bragg reflecting (DBR) mirrors in vertical-cavity surface-emitting lasers.[1] The high contrast grating offers a simpler geometry than the large stacks required of DBRs. Zhou et al.[2] proposed a novel hollow-core waveguide structure that uses such high-contrast gratings. Their simulations showed ultra-low loss properties. The realization of the hollow-core waveguide with a high-contrast grating (HWHCG) would allow for a semiconductor-based, chip-scale waveguide that would exhibit low loss, similar to that of optical fiber. The waveguide proposed by Zhou et al. would require three-dimensional (3D) processing of sub-wavelength scale features of the structure shown in figure 1a. However, using existing semiconductor processing techniques, it will be very difficult to fabricate such a 3D structure. It would likely require a complex process with the undesirable use of wafer-bonding, deposition, and regrowth techniques. Our processing method can be used to fabricate a simplified 3D photonic crystal (PhC) structure below the surface of a Si wafer, which is shown schematically in figure 1b. Although slightly different than the structure in figure 1a, it contains the necessary features for light propagation.

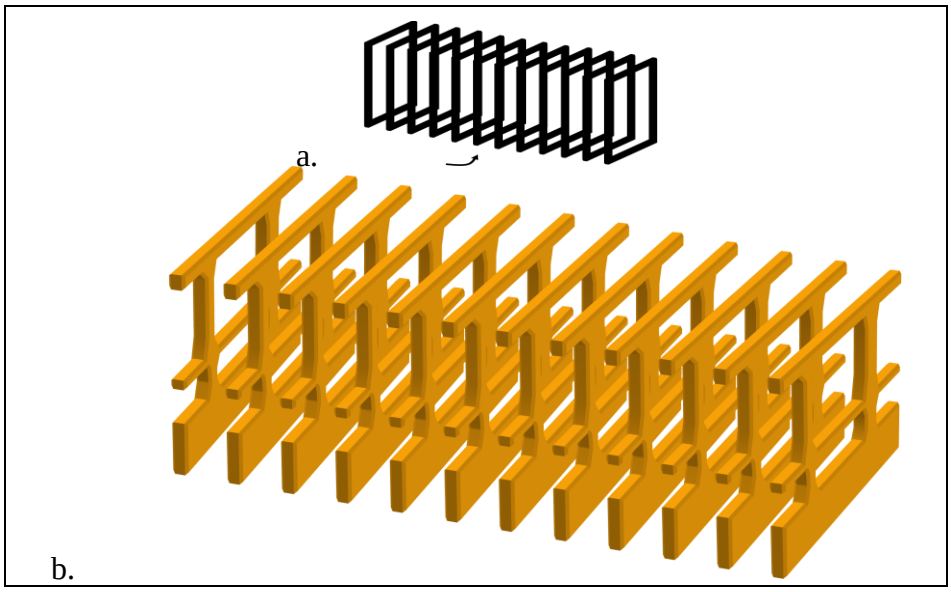

Figure 1. (a) Structure of the ultra-low loss HWHCG and (b) schematic of a hollow-core high-contrast waveguide using our modified Bosch etch process.

[1] Chang-Hasnain, C. J. Tunable VCSEL Using High Contrast Grating. *Conference on Lasers and Electro-Optics/International Quantum Electronics Conference*, OSA Technical Digest (CD), Optical Society of America, 2009, paper CThB1.

[2] Zhou, Y.; Karagodsky, V.; Sedgwick, F. G.; Chang-Hasnain, C. J. Ultra-Low Loss Hollow-Core Waveguides Using High-Contrast Gratings. *Conference on Lasers and Electro-Optics/International Quantum Electronics Conference*, OSA Technical Digest (CD), Optical Society of America, 2009, paper CFV7.

2. Procedure

In order to fabricate 3D structures, e.g., the HWHCG, below the semiconductor surface using our etch method, it is necessary to be able to control the width of the etch profile while maintaining vertical sidewalls. The standard Bosch etch process[3] allows high-aspect ratio etches in Si with vertical sidewalls. By modifying the Bosch process, we are able to obtain high-aspect ratio etches with etch profiles that have varying widths. We have been able to obtain etch sidewall profiles with three regions of varying widths, each having vertical sidewalls.

The Bosch etch process uses a repetition of three steps to achieve a high-aspect ratio etch in Si with vertical sidewalls. In its most basic form, the Bosch process has a first step where the polymer conformally passivates the sample with a patterned mask—in our case, an e-beam resist. The second step is a directional etch to remove polymer that is on the bottom of the e-beam resist features to expose the Si, while maintaining protective polymer on the sidewalls of the trench. Finally, an isotropic Si etch step is performed to remove a thin layer of silicon. The key to the Bosch process is the restarting of the three-step loop once the sidewall polymer is eroded by step three, the Si etch. By repeating this three-step cycle, one can etch a deep trench in Si with vertical sidewalls. We modified the standard Bosch process to achieve a wider core region in our etch profile by increasing the times for the first step (polymer deposition) and third step (silicon etch). The increase in the polymer deposition time provides sidewall protection for the wider lateral etch of the core's second region. The process for the first and third regions of the etch is the standard Bosch process.

3. Results

Figure 2 shows a scanning electron microscope (SEM) image of such etch cross-sectional profiles performed in a 300-nm-wide line with features defined by a ZEP 520 e-beam resist. The three regions of the profile are a narrow first region, a wider second region, and then a narrow third region that is as wide as the first region. This type of etch profile, if performed in two lines in proximity to each other, will form one of the rings in the HWHCG structure. Regions 1 and 3 of the etch profile will form the frame of the ring, and region 2 of the lines will etch laterally into each other forming the "hollow-core." For a grating width of 600 nm, the second region of the etch needs to etch to a width of approximately 600 nm so that adjacent rings open up. It is also important that the first and third regions of the etch have the same width, as they form the ring frame of the waveguide. The samples were etched in a Unaxis VLR 700 ICP system.

[3]Laermer, F.; Schilp, A. of Robert Bosch GmbH. Method of Anisotropically Etching Silicon, U.S. Patent No. 5501 893.

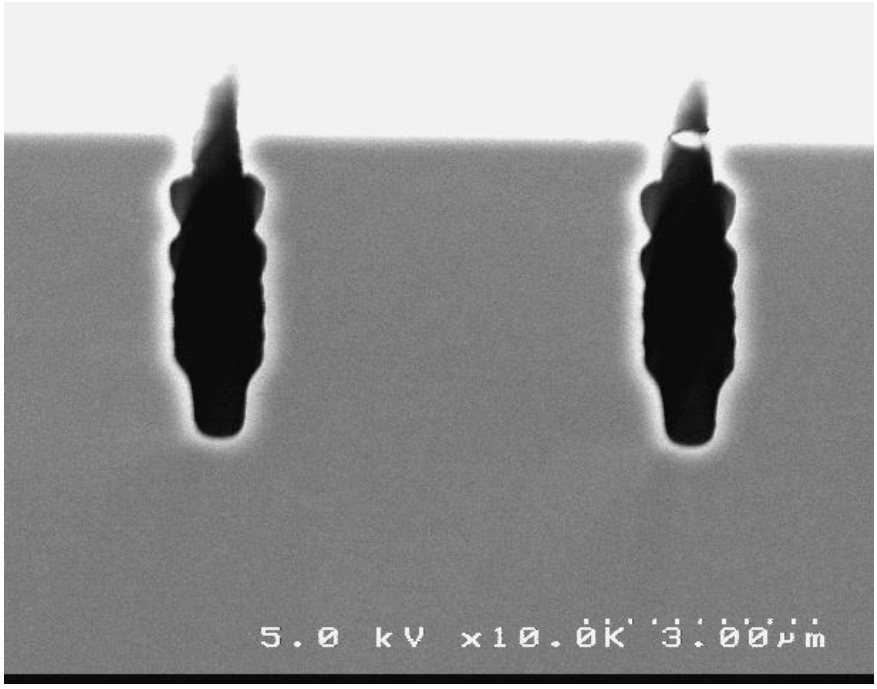

Figure 2. Etch profile of test lines approximately 300 nm wide using our modified Bosch etch.

By combining this variable-width vertical trench etching technique with a two-dimensional (2D) mask having periodic gap lines that have wide and narrow regions, we can create the desired 3D HWHCG structure as shown in figure 1. Figure 3 shows a top-view image of an etch performed for fabrication of an array of five hollow-core waveguides. The e-beam resist has been stripped using oxygen plasma, but the pattern etched in Si is the layout of the top mask pattern. The period of the grating is 600 nm. The narrow line region from the top view was completely undercut by the etch to form the rings, but the wider rectangular features in the pattern were not completely undercut. These features form vertical posts that become the vertical high contrast grating claddings of the waveguide.

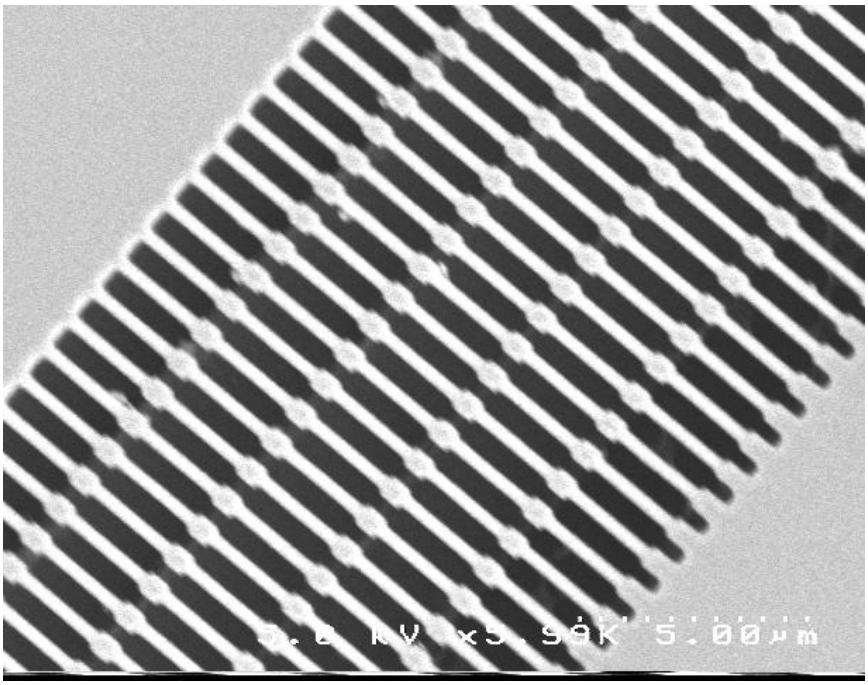

Figure 3. Top view of etched Si wafer. This structure is an array of five waveguides.

Figure 4 shows a cross-sectional view of the structure after cleaving. Some roughness can be seen along the posts, as well as an unwanted artifact in the core region of the waveguides. A short oxidation and etch in buffered oxide etch (BOE) should remove these features. The sample was fabricated on an SOI wafer where a sacrificial silicon-oxide layer is located under the bottom cladding layer made by the high contract gratings. The BOE chemical etch can also remove the silicon-oxide layer under the waveguide so that the waveguides are "sitting" on a layer of air.

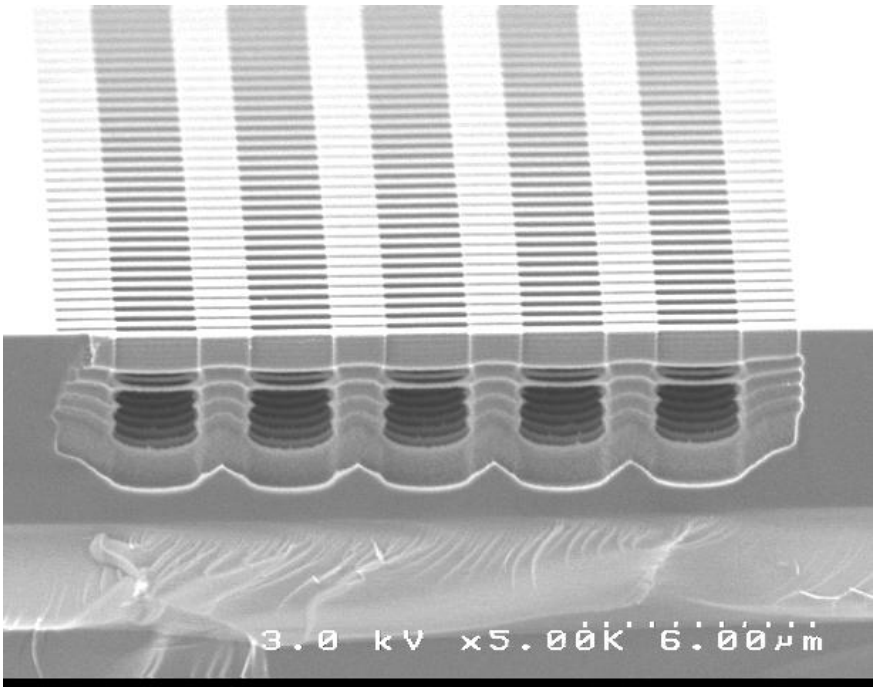

Figure 4. Cross-sectional view of waveguides fabricated in an SOI wafer.

4. Conclusions

In conclusion, we have demonstrated a method for fabricating HWHCGs in silicon. This method allows for a low-loss waveguide alternative to optical fiber that can be monolithically integrated with semiconductor components. Currently, optical fiber cannot be monolithically integrated with semiconductor photonic integrated circuit (PIC) and conventional semiconductor waveguide devices have high loss. Many analog optical and RF-photonic systems need to use optical fiber as a high Q device or time delay device. Our single-etch processing method not only makes the integration of fiber-like waveguides with PIC possible, it also increases the likelihood that fabrication on a large scale will have low cost and higher yield, thus making it a practical component in Army's RF and optical systems, such as opto-electronic oscillators and optical controlled phased array antenna, that require high bandwidths and greater immunity to electromagnetic interference. This method can also be applicable to digital communication and control systems that require buffers.

List of Symbols, Abbreviations, and Acronyms

2D	two-dimensional
3D	three-dimensional
BOE	buffered oxide etch
DBR	distributed Bragg reflecting
HWHCG	high-contrast grating
PhC	photonic crystal
PIC	photonic integrated circuit
SEM	scanning electron microscope
Si	silicon
SOI	silicon on insulator

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